UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,167	08/08/2003	Marc Tremblay	SUN-P9329-MEG	2957

57960 7590 08/18/2006

SUN MICROSYSTEMS INC.
C/O PARK, VAUGHAN & FLEMING LLP
2820 FIFTH STREET
DAVIS, CA 95618-7759

EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/637,167	TREMBLAY ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed May 02, 2006 in response to PTO Office Action mailed March 24, 2006. The Applicant's remarks and amendments to the claims were considered with the results that follow.

2. In response to the last Office Action, claims 1, 15, and 29 have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-29 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 15 and 29 have been fully considered but they are not fully persuasive. Rajwar fails to explicitly teach an explicit instruction to start transactional execution.

4. Applicant admits that Rajwar teaches eliding lock-acquire operation and speculatively executing a critical section of code. In order to elide a lock-acquire operation, the invention of Rajwar observes "load and store sequences and values read and to be written". The "values read and to be written" by store/load instruction can be interpreted as analyzing respective instruction. Thus, Rajwar does teach analyzing the store instruction. Applicant argues that invention of Rajwar is implemented entirely in microarchitecture without instruction set support system level modifications but the meaning was "e.g. no coherence protocol changes are required and is transparent to programmers". According to Tanenbaum (Structured Computer Organization),

microarchitecture level is a register level implementation and programs written in Instruction set architecture (ISA) are control by this level (see pages 5,6). Thus, the method of Rajwar can be machine language independent.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on April 14, 2006 has considered by the examiner.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6,10-14, 15-20, 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar et al. (Speculative Lock Elision; ACM/IEEE International Symposium; Dec. 2001) (Rajwar herein after) and Jim Gray (The Transaction Concept: Virtues and Limitations) and further in view of Oplinger et al. (Enhancing Software Reliability with Speculative Threads (provided as IDS by the applicant)).

As per claims 1,15 and 29, Rajwar teaches a method of monitoring store instruction to support transactional execution of process, comprising:

encountering a store instruction during transactional execution of a block of instructions in a program (page 298, column 1, lines 1-2, taught as filter is used to

determine candidate load/store pairs for speculative execution), wherein changes made during the transactional execution are not committed to the architectural state of a processor until the transactional execution successfully completes (taught as critical section is executed speculatively and the results are buffered. If atomicity is not violated the results are committed (page 297, column 1, paragraph 2). Transactions as taught by Jim Gray, either happens or it does not (page 144, column 2), thus Rajwar explicitly teaches transactional execution).

Monitored store instruction is not well known to ordinary skilled in the art, hence the definition from the specification of the present application as understood by the examiner as the instruction need to be monitored for interference during the speculative execution of the critical section. Rajwar teaches store instruction and monitors the interferences by other processor (page 299, section 5.1 lines 1-2 for initiating store instruction, and section 5.3 for monitoring of interference) thus Rajwar inherently teaches generating monitored store instruction. Rajwar also teaches store marking of the cache lines (page 298, section 4, paragraph 2-3). Rajwar teaches analyzing a store instruction (page 297, col. 2, par. 2, taught as "load/store sequences and the values read and to be written are observed, this can be broadly interpreted as "analyzing").

Rajwar fails to teach selectively monitoring the store instruction, but Rajwar states that limited resources may force a miss-speculation if either there is not enough buffer space to store due to finite cache size and the number of unique cache lines modified (marked for interference detection) exceeds the write-buffer size (page 300 column 1). Jim Gray teaches transactions can be categorized as unprotected, protected

and real. Jim Gray also teaches transactions of unprotected data need not be undone or redone if the transaction must be aborted (page 145 column 1).

It would have been obvious to one having ordinary skilled in the art at the time of the invention to have modified the transactional execution system of the Rajwar using the teachings of Jim Gray by generating selectively monitored store instructions to reduce the marking of the cache lines and hence increase the write-buffer size (limitations of Rajwar as explained above). As Jim Gray implicitly teaches that all transaction need not be monitored for the interference because unprotected transactions need not to be redone.

Rajwar and Jim Gray fail to teach, an explicit start transactional execution instruction. Oplinger teaches a "try" instruction to start transactional execution (see page 187, col. 2, line 13). It would have been obvious to one having ordinary skill in the art at the time of the invention to use "try" instruction to start transactional execution in the system Rajwar and Jim Gray because encountering "try" instruction, indicates the start of transactional execution and all the side effects of speculative execution are buffered to guarantee the memory is restored to its state just before the "try" instruction (see Oplinger, page 187, col. 2, lines 5-17).

As per claims 2,5,16 and 19, it would have been obvious to one having ordinary skill in the art at the time of the invention would have generated monitored store instruction towards protected data to monitor interference from other processor as per claim 1 and 15. Also one having ordinary skill in the art would have generated unmonitored store instruction for unprotected data.

As per claims 3 and 17, protected data structure as well known to one having ordinary skill in the art means, the data that needs to be protected from other processors by means of locking or using semaphores. As such one having ordinary skill in the art at the time of the invention would have monitored the store operations associated with protected data for interference.

Regarding claims 4 and 18: A heap is a portion of a memory reserved for a program to use for the temporary storage of data structures. So any processor can access data from heap and hence the store instruction associated with the heap must be monitored for interference.

Regarding claims 6 and 20: Op code (as defined in Microsoft Computer Dictionary on page 378) is a portion of the part of machine language instruction that specifies the type of instruction and the structure of the data on which it operates. Accordingly, one having ordinary skill in the art at the time of the invention would have used the op code to distinguish between the monitored or unmonitored instruction and corresponding data structure.

As per claims 10 and 24, Rajwar teaches that if a data conflict occurs the atomicity cannot be guaranteed and such execution is not retired architecturally (i.e. changes are not committed) (page 297, column 1, lines 4-10) and if atomicity is not maintained then processor can try to execute the algorithm again (page 297, column 1, lines 28-30).

As per claims 11 and 25, Rajwar teaches that if atomicity was not violated than commit the speculative state and exit speculative critical section (page 297, column 1, lines 19-23).

As per claims 12 and 26, Rajwar teaches that the atomicity is maintain by read-modify-write primitives (page 296, column 1, section 2.2) and interfering data access under such primitives are store by another processor to the store-marked cache line or load or store by another processor to a cache line that has been store marked (page 296, section 3.2, lines 13-19).

As per claims 13 and 27, Rajwar teaches the cache line is store-marked in the cache level closest to the processor where cache lines are coherent (page 298, column 2, section 4, paragraph 2-3).

Claims 14 and 28 are rejected as same rationale applied to claims 1, 12, 15 and 26 above. As per claims 1 and 15 a store-marked cache line indicates that the instruction should be monitored for interference and the changes are committed until successful execution of the transaction and as per claims 12 and 26, one of the method to check the atomicity is to monitor the loads and stores from other process to cache marked lines and stores by same process to cache marked line. Thus, Rajwar implicitly teaches that cache-marked cache line indicate monitoring of load/store by other process as well as store by same process.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7-9 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajwar et al. (Speculative Lock Elision; ACM/IEEE International Symposium; Dec. 2001) (Rajwar herein after), Jim Gray (The Transaction Concept: Virtues and Limitations), Oplinger et al. (Enhancing Software Reliability with Speculative Threads) and Microsoft Computer Dictionary (Fifth edition, published in 2002) as applied to claims 1-6 and 15-20 above, and further in view of Gaskins et al. (US 6,618,311 B2) (Gaskins herein after).

As per claims 7-9 and 21-23, Rajwar, Jim Gray and Oplinger combined teaches a method of generating monitored or unmonitored store instructions as applied to claims 1-6 and 15-20 above, but fail to teach determining whether the store instruction is monitored store instruction involves examining an address associated with the store instruction. Gaskins teaches method of caching using a Translation Lookaside Buffer (TLB) (see abstract). According to Gaskins TLB performs a lookup of the virtual page number and performs the comparison of base addresses (column 1, lines 64-67 and column 2, lines 1-11). Gaskins also teaches that microprocessor provides a mechanism for mapping a physical address range of a memory type and memory address ranges. The memory type specifies the cache attributes associated with the address range,

such as whether the address range is cacheable or uncacheable, write-back or write-through, writeable or write-protected and these attributes controls the whether the specified address range supports out-of-order or speculative accesses (column 2, lines 38-52).

It would have been obvious to one having ordinary skill in the art at the time of the invention would have used the teachings of Gaskins in the systems of Rajwar and Jim Gray to generate monitored store instruction for certain specified address ranges.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

Reginald D. Bragdon

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100